Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently Amended) A multi-mode bi-directional communications device, comprising:

a diplexer having a high-pass filter coupled between a first signal port and a second signal port, a low-pass filter coupled between the first signal port and a third signal port;

a digitally operable switch, connected in signal communication with the low-pass filter, responsive to signals from a microprocessor; and

a notch filter selectively coupled to the low-pass filter by the digitally operable switch in response to indicium of a desired spectral region,

wherein said notch filter comprises only a plurality of inductors and a plurality of PIN diodes, each of the plurality of inductors having a first end and a second end, each of the plurality of inductors connected in parallel with a respective one of the plurality of PIN diodes at the first end and a common control node at the second end.

2. (Original) The device of claim 1, further comprising upstream processing circuitry and downstream processing circuitry coupled to said diplexer.

3. (Previously Presented) The device of claim 2, wherein the downstream processing circuitry comprises:

a tuner;

a demodulator;

a first surface acoustic wave (SAW) filter selectively coupled between said tuner and said demodulator; and

a second SAW filter selectively coupled between said tuner and said demodulator.

4. (Original) The device of claim 3, wherein the first SAW filter has a bandwidth of 6MHz and the second SAW filter has a bandwidth of 8MHz.

5. (Original) The device of claim 3, further comprising at least one selector for selectively coupling the first SAW filter and the second SAW filter between the tuner and the demodulator.

6. (Original) The device of claim 3, wherein said high-pass filter is coupled to said tuner.

7. (Original) The device of claim 1, wherein said high-pass filter passes signals greater than 88MHz.

8. (Previously Presented) The device of claim 2, wherein said upstream processing circuitry is selectively coupled to one of said low-pass filter and said low-pass filter in conjunction with said notch filter.

9. (Previously Presented) The device of claim 1, wherein the low-pass filter nominally passes signals less than 65MHz, and passes signals less than 42MHz when the notch filter is coupled thereto.

10. (Cancelled)

11. (Previously Presented) The device of claim 1, wherein the digitally operable switch is selected from a group consisting of a transistor, and a PIN diode.

12. (Previously Presented) The device of claim 1, wherein said device is selected from a group comprising a cable modem and a satellite terminal.

13. (Original) The device of claim 1, wherein said device supports multiple standards selected from the group consisting of the North American Data Over Cable Service Interface Specifications (DOCSIS) or the European DOCSIS standards.

14. (Currently Amended) A diplexer, comprising:

a high-pass filter coupled between a first signal port and a second signal port;

a low-pass filter coupled between the first signal port and a third signal port;

a digitally operable switch, connected in signal communication with said low-pass filter, responsive to signals from a microprocessor; and

a notch filter, selectively coupled to the low-pass filter by the digitally operable switch in response to indicium of a desired spectral region,

wherein said low-pass filter comprises a first set of inductors connected in series between said first and third signal ports, each of said first set of inductors being coupled to ground via a respective capacitor from a set of capacitors forming thereby a plurality of single pole filter elements, a portion of said first set of inductors being bypassed by a subset of the set of capacitors, the portion consisting of any of the first set of inductors which are connected to said notch filter via any of the capacitors in the subset of capacitors,

wherein said notch filter comprises a second set of inductors, where each inductor is respectively coupled between a particular one of capacitors in the subset of capacitors and ground, and

wherein a subset of the first set of inductors are directly connected to ground via only the respective capacitor from the set of capacitors, the subset of the first set of inductors consisting of any inductors in the set of inductors that are directly coupled to any capacitors in the set of capacitors that are excluded from the subset of capacitors.

15. (Cancelled)

16. (Original) The diplexer of claim 14 wherein said high-pass filter comprises:

a plurality of capacitors connected in series between said first and second signal ports, each of said capacitors being coupled to ground via serially coupled circuit elements forming thereby a plurality of single pole filter elements, each of said serially coupled circuit elements comprising a capacitor and inductor.

17. (Cancelled)

18. (Previously Presented) The diplexer of claim 14, wherein the digitally operable switch is selected from the group consisting of PIN diodes, and transistors.

19. (Previously Presented) The diplexer of claim 15, wherein the digitally operable switch comprises:

a plurality of PIN diodes respectively coupled in parallel with said second plurality of inductors, wherein said PIN diodes are adapted for connection to a control signal from the microprocessor for selectively biasing the PIN diodes to couple and decouple the notch filter to the low-pass filter.

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) The diplexer of claim 14, wherein said notch filter comprises a plurality of inductors and a plurality of ~~pin~~ PIN diodes, each of the plurality of inductors having a first end and a second end, each of the plurality of inductors connected in parallel with a respective one of the plurality of ~~pin~~ PIN diodes at the first end and a common control node at the second end.